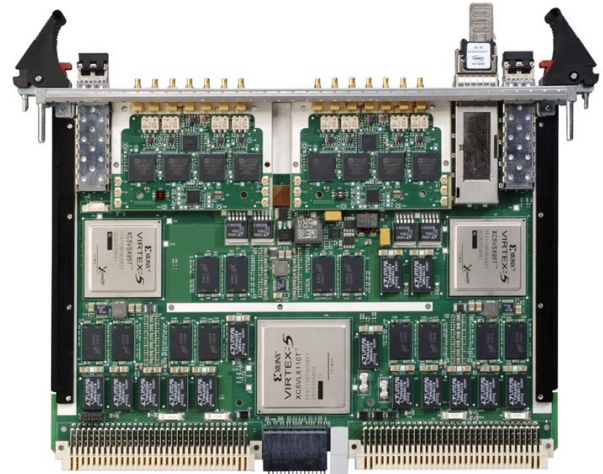


Charon-V5 VXS

Maximum FPGA Density
 Combined with High Performance
 Mixed Signal Technology.
 Without Compromise.

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Features

Benefits

| | |
|---|---|
| Eight Channels: Eight 14-bit DAC Outputs at 1.2 GSPS Each | Multichannel Output in A Single Slot |
| Sample Accurate Synchronization Across Multiple Boards | Supports High Channel Count Applications Such as Beam Steering With up to 144 Channels in a Single VXS chassis. |
| First COTS Product to Achieve This Level of Analog Signal Performance. | Unprecedented Capability for Developers Requiring Ultra Wide Band Signal Generation |
| Six Digital IO Channels Running at Up to 3.75 Gb/s Using One QSFP and Two SFP+ Front Panel Connections | Flexible Data Movement Across the Front Panel For Use in Standard VME64 Environments |
| Dual 4x Full Duplex VXS Links and Two Full Duplex VITA 41.6 Ethernet Links | Enhanced VXS Capability |
| Three Xilinx Virtex®-5 FPGAs: LXT, SXT or FXT for Each Location | Unmatched FPGA Processing Per Channel |
| Three GB DDR3 SDRAM Memory, (one GB per FPGA as two, 512 MB, 64-bit banks) | Large Memory Resources for Application Flexibility |
| Advanced Temperature & Current Monitoring | Protection From Damage and Usable in Customer Applications |
| Comprehensive Developer's Kit Provided Including FPGA Interface Cores, QuiXtart FPGA Utilities, Software and Reference Design | Faster Application Development |
| Convection or Conduction Cooled Options | Ruggedization Designed in For Demanding Deployed Applications |

Overview

The QuiXilica Charon-V5 VXS is a 6U ANSI/VITA 41 (VXS) compliant high-speed waveform generator board combining high density FPGA processing with eight 14-bit D/A output channels at 1.2 GSps.

By employing three Xilinx Virtex®-5 FPGAs, the Charon-V5 offers unmatched FPGA processing density per channel making it ideal for high channel count signal processing in applications such as RADAR, signals and electronic intelligence (SIGINT / ELINT), and Electronic Warfare (EW).

Charon-V5 Reduces System Size by 30%

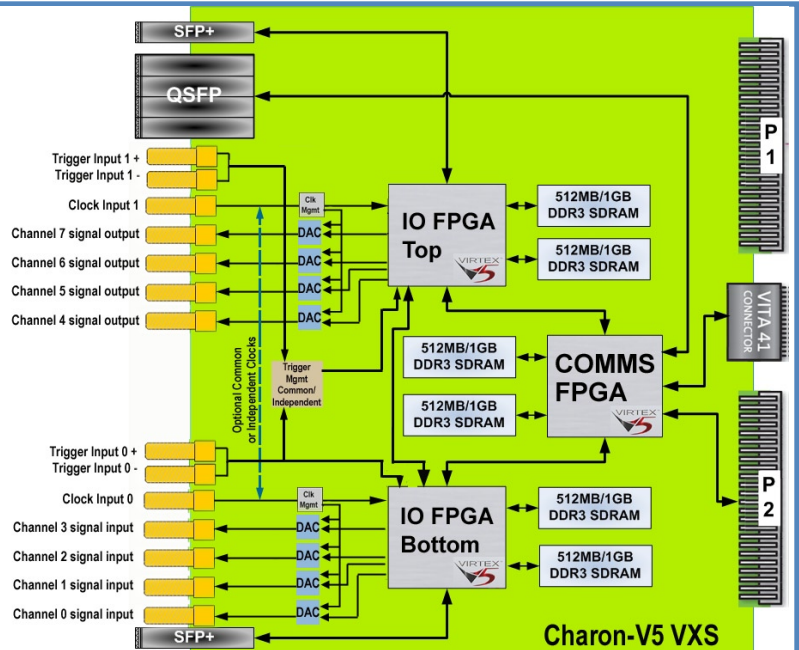
Many advanced signal processing applications are based on antenna array processing and require large numbers of channels and distributed signal processing. The architecture of the Charon-V5 combines eight analog output channels with three Xilinx Virtex-5 FPGAs, providing up to 2,336 DSP slices and 1.285 TeraMAC/s of signal processing, equivalent to 61% of a Xilinx Virtex-5 SX95T device per input channel. For high channel count requirements such as beamforming, direction finding, jamming or anti-jam / interference cancellation, common in Radar, SIGINT, communications, and EW applications, Charon-V5 provides both the highest processing density per channel and per 6U slot, reducing total size, weight and power for many systems.

For example, in a phased array processor system with 20 I/Q inputs, where one FPGA is assigned to process data for each I/Q input channel, a traditional PMC or XMC based architecture would require 10 or even 20 slots depending on SBC selection and FPGA requirements. The same system can be implemented in 7 slots using the Charon-V5 VXS, using less space and power but still providing the same number of channels and 40% more FPGA processing capability than a 10 slot XMC-based system with 20 XMC modules using SX95T FPGAs.

The Charon-V5 features high bandwidth, low latency interconnect paths between its FPGAs which have been carefully specified to ensure that data from any analog channel can be broadcast to all FPGAs to support processing that relies on simultaneous access to data from all channels. This offers significant throughput advantages for a range of advanced multi-channel processing algorithms found in applications such as Direction Finding, STAP (Space Time Adaptive Processing) Radar and Synthetic Aperture Radar (SAR) Image Formation.

The Charon-V5 is available for a wide range of operating environments, including commercial grade, rugged air and conduction cooled to support deployed applications such as unmanned airborne, naval and ground vehicles. For more information see the Rugged Data Sheet.

Charon-V5 Configuration



Tekmicro offers a broad range of Xilinx Virtex-5 based streaming I/O and FPGA processing solutions for both analog and digital I/O in a range of form factors.

Charon-V5 VXS Details

Front Panel High Speed Serial IO

Two SFP+ sites and one QSFP site are provided on the front panel which utilize standard fiber optic or 1000BaseT modules providing physical layer support for standard protocols such as Gigabit Ethernet, Serial FPDP (ANSI VITA 17.1 & 17.2), and Fibre Channel.

Virtex-5 FPGAs

Xilinx Virtex-5 FPGAs are the heart of the Charon-V5. The FPGAs interface with the DACs, memory and I/O resources providing the user with a platform for implementing high performance real time processing. The Charon-V5 is typically configured with two SX95T FPGAs and an LX110T. Developers can alternatively select an LX220T, SX240T, or FX100T FPGA to match resources to the application. All FPGAs are interconnected by wide parallel LVDS busses or high speed serial lanes using FPGA embedded MGTs.

VXS Backplane High Speed Serial IO

The Charon-V5 can be used as a VITA 41.0 payload card. Up to eight high speed serial links of up to 3.125 Gb/s full duplex data rates are supported via the VITA 41.0 MultiGig RT2 P0 connector. Custom or standard communication protocols can be run over these links by providing appropriate firmware in the FPGA.

QuiXstart FPGA Configuration

A number of options are available for configuring the FPGA on the Charon-V5. A JTAG connection is available to allow users to configure the FPGA via standard Xilinx development tools. On board flash is available and can configure the FPGA on power up. Tekmicro's QuiXstart tool supports flexible configuration of the FPGA through a Gigabit Ethernet link from a remote server after a power up or reset event.

DACs

Eight channels of up to 1,2 Gbps, 14-bit resolution digital to analog conversion is provided using the Analog Devices' AD9736. The outputs are single-ended, AC coupled. Maximum full scale output is 4.5 dBm (1.1 V p-p) into 50 ohms. The layout has been carefully designed to ensure phase matching of the clock across all channels. A separate single 16 bit wide bus connects the SXT95T/LX110T FPGA directly to each DAC. The layout has been designed to ensure phase matching of the clock across all output channels. Trigger input connections are provided on the front panel to allow the hardware to be employed in a variety of Radar and EW scenarios.

Memory

The Charon-V5 has two independent banks of onboard double data rate (DDR3) SDRAM for each FPGA, providing a capacity of 512 MB in each bank, and 1 GB total per FPGA. The on board memory can be clocked at rates up to 400 MHz, 800 MHz double data rate.

System Monitoring

The Charon-V5 board includes facilities to monitor current and temperature at various points on the board. Current monitoring of all main power rails is available. Die temperature monitoring of the three FPGAs and temperature monitoring of three locations on the PCB is also available. This allows a first level of protection to be implemented when the Charon-V5 is operating in a variety of different environmental scenarios. The output from the sensors will also be available to users through the "COMMS FPGA" firmware. The condition monitoring peripherals share an I2C bus along with the I2C bus from the COMMS FPGA to the QSFP module.

PERFORMANCE SPECIFICATIONS

Front Panel Analog Signal Outputs

Quantity: 8 DACs SSMC Connectors

Sampling Rate: 1.2 GSPS

Resolution: 14-bits

Type: Analog Devices AD9736

Type: Single ended

DAC Full Scale Output: 4.5 dBm

Bandwidth: 1st Nyquist

Front Panel High Speed Serial Interface

2x SFP+ Ports: Providing (2) digital high-speed serial I/O connections. Range of standard protocols, including Gigabit Ethernet and FibreChannel. Firmware supplied at additional cost.

1x QSFP Port: A quadruple SFP connector of (4) independent lanes of digital high-speed serial I/O. The lanes may be bonded together. The port supports a range of standard protocols: Gigabit Ethernet, FibreChannel and 10-Gigabit Ethernet (via 4-lane XAUI). Firmware supplied at additional cost.

Front Panel Trigger Inputs

Quantity: 1 or 2 via (2 or 4) SSMC Connectors

Standalone: Optional Independent Trigger inputs for each group of four DACs.

Master/Slave: Select Trigger MASTER, SLAVE provides common trigger for all eight DACs

External Clock

Quantity: 1 or (2) via (2) SSMC Connectors

Single ended 50Ω terminated

Input Power Range: 6 dBm (min) to 8 dBm (max)

Operating Modes: Clock Standalone / Master/Slave.

Standalone: Use independent clock inputs for each group of four DACs

Master/Slave: Common clock distributed to all eight DACs

Contact factory for additional performance details.

Memory

DDR3 SDRAM (2 banks per FPGA)

Size: (STD): 512 MB per bank, 1 GB total per FPGA

Bus: Width: 64 bits

Speed: 400 MHz, 800 MHz double data rate

JTAG Port

Access to Virtex-5 FPGAs is available via custom JTAG cable assembly that interfaces with the JTAG programming cable.

Size: Standard 6U VMEbus board, single slot; PCB: 160mm (6.3") x 233.5mm (9.2") Option: VXS P0 connector for backplane I/O

Power: +5V, +3.3V, +12V from VME64 backplane. Power consumption is dependent on customer application. Power estimating tools are available on request.

Rugged Options:

Tekmicro products operate effectively in laboratory, rugged air-cooled, and rugged conduction-cooled environments to meet the needs of R&D and deployed applications.

Commercial products are intended for use in application development and benign operating environments. Rugged Level 2, convection cooled, products are intended for harsh environments with more demanding temperature, humidity, shock, and vibration requirements. Rugged Level 3, conduction cooled, products provide wider operating temperatures and increased capabilities for shock, vibration, and humidity for extreme operating conditions.

For complete specifications refer to the Rugged Data Sheet.



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